

## Lecture 3

# Understanding op-amp specifications

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# What you should know already?

## C-E Amplifier Revisited Quiescent Analysis

- KVL on input side

$$V_{BIAS} = I_B R_B +$$

and  $V_{BE} \approx 0.7$  V,  $I_E =$

$$\Rightarrow I_E \approx \frac{(V_L)}{[R_E]}$$

- As before:

$$V_F = I_F R_F$$

where we have used  $I_S \propto A$ , and

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## INPUT SIDE

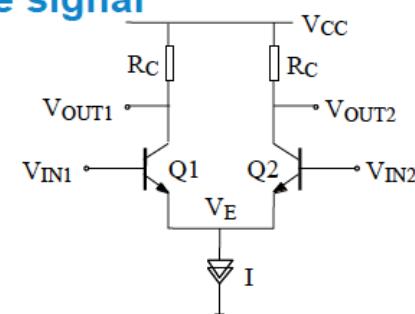


- For transistors identical apart from

$$I \approx I_R$$

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## The Differential Pair – large signal



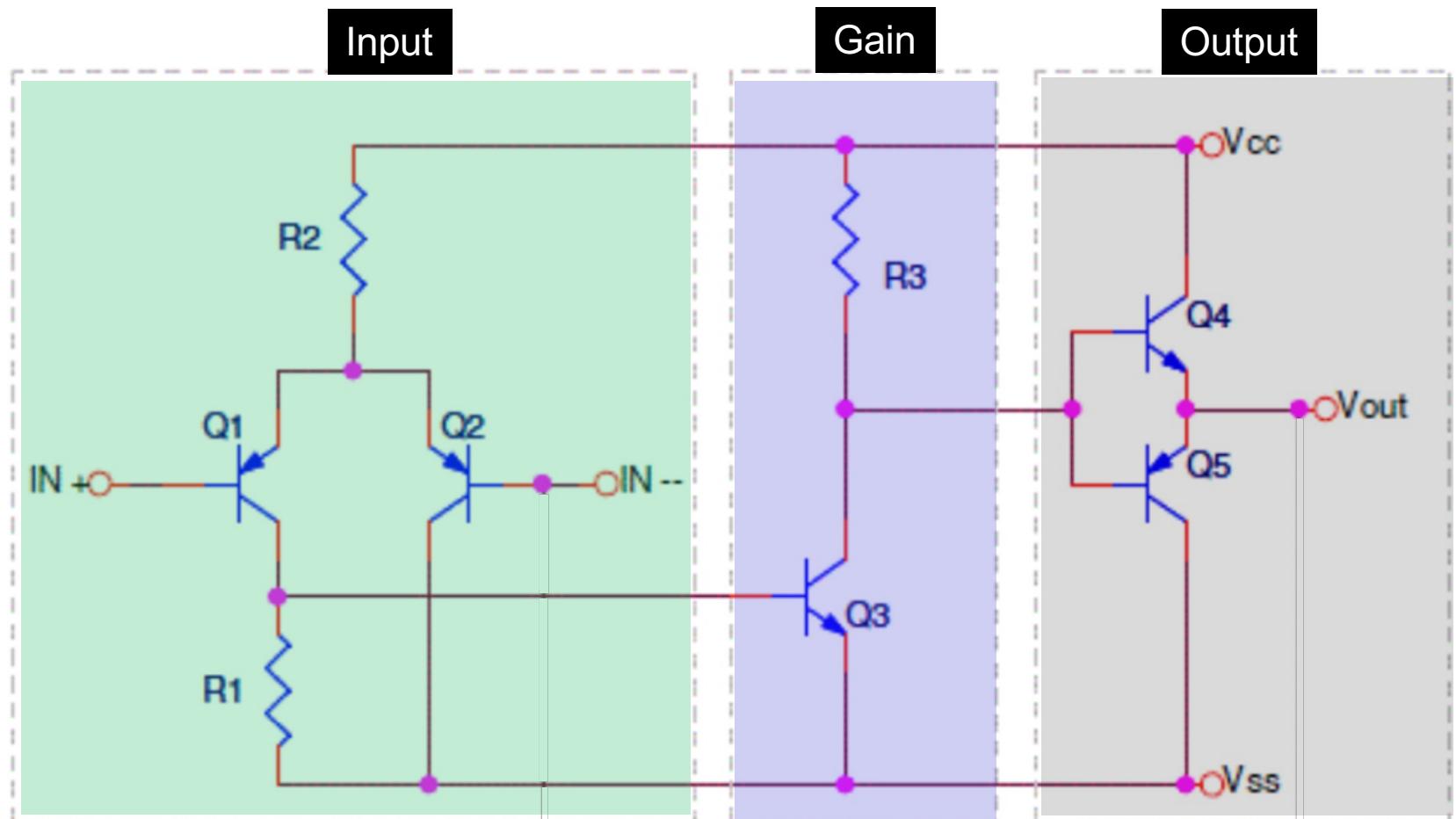
- If transistors are matched, then:

$$I_{C1} = \frac{I}{1 + \exp(-V_D/V_T)} \quad I_{C2} = \frac{I}{1 + \exp(V_D/V_T)}$$

$V_D = (V_{IN1} - V_{IN2})$  is the DIFFERENTIAL INPUT VOLTAGE

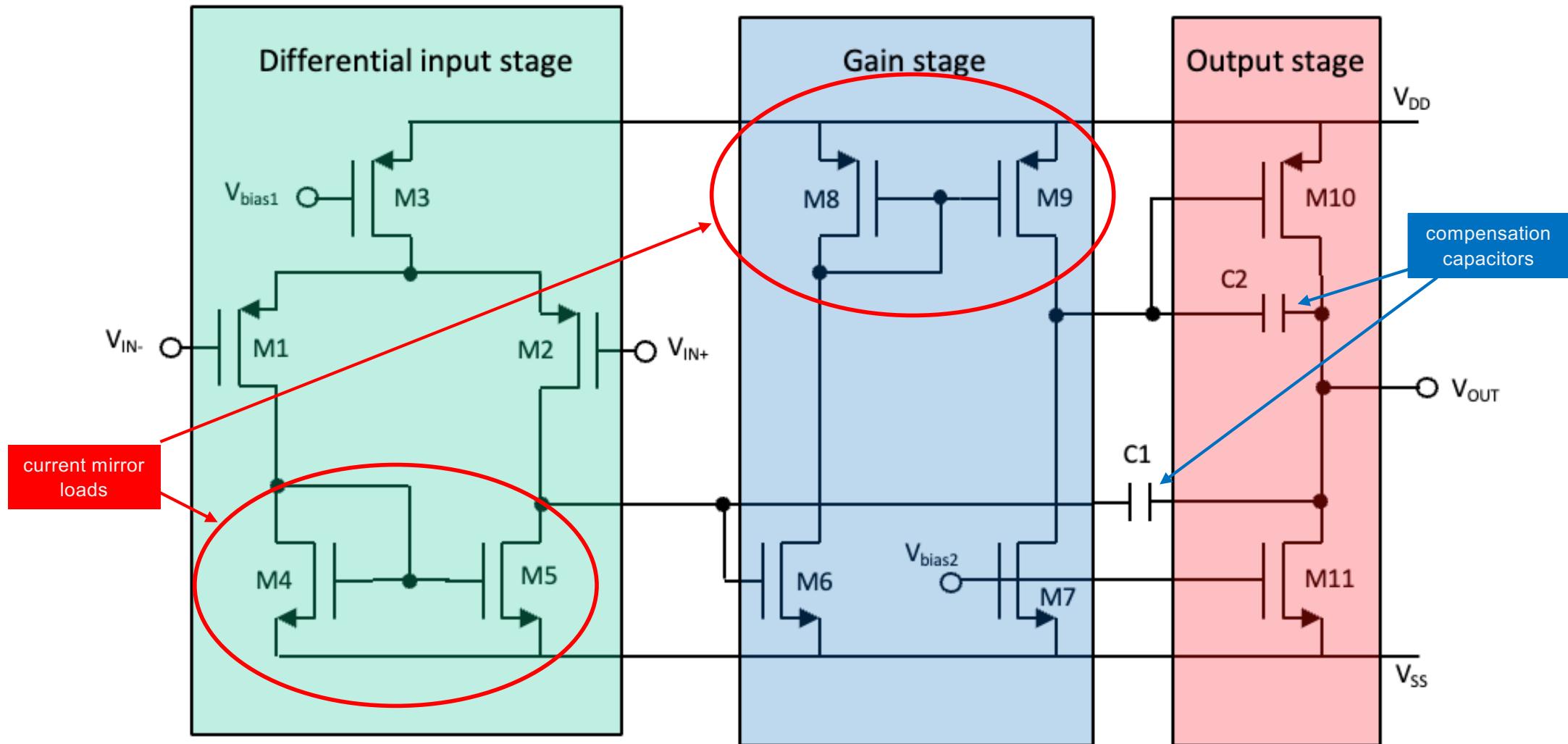
# Inside a typical BJT op-amp

- ❖ Three stages architecture:
  1. **Differential input stage** – long-tail pair (Yr 1 Circuits part 2, adc\_9, slides 8-14)
  2. **Voltage gain stage** – common emitter amp (adc\_6, slides 3-7)
  3. **Output drive stage** – push-pull circuit



# Inside a typical MOSFET op-amp

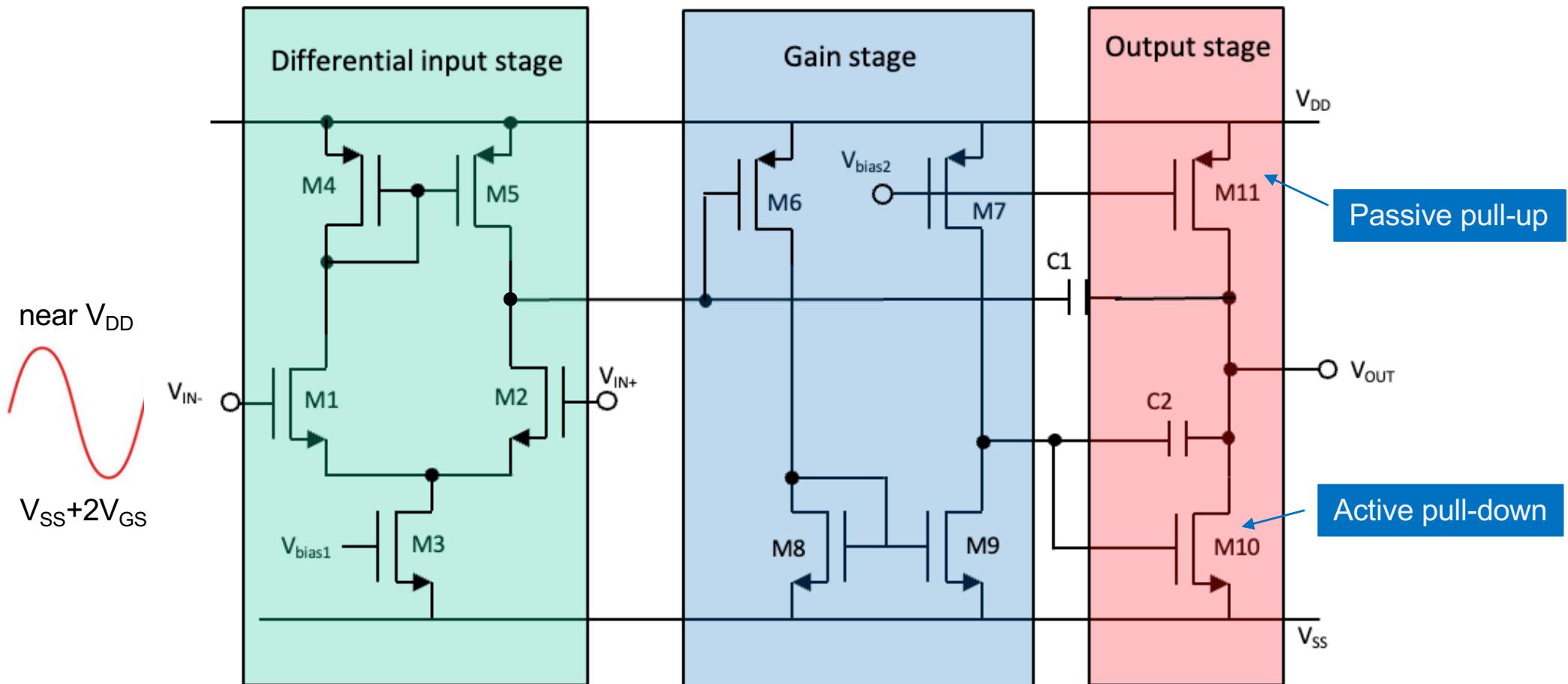
- ❖ Early MOSFET op-amp follows similar architecture to the BJT version.



# n-type input MOSFETs but not rail-to-rail

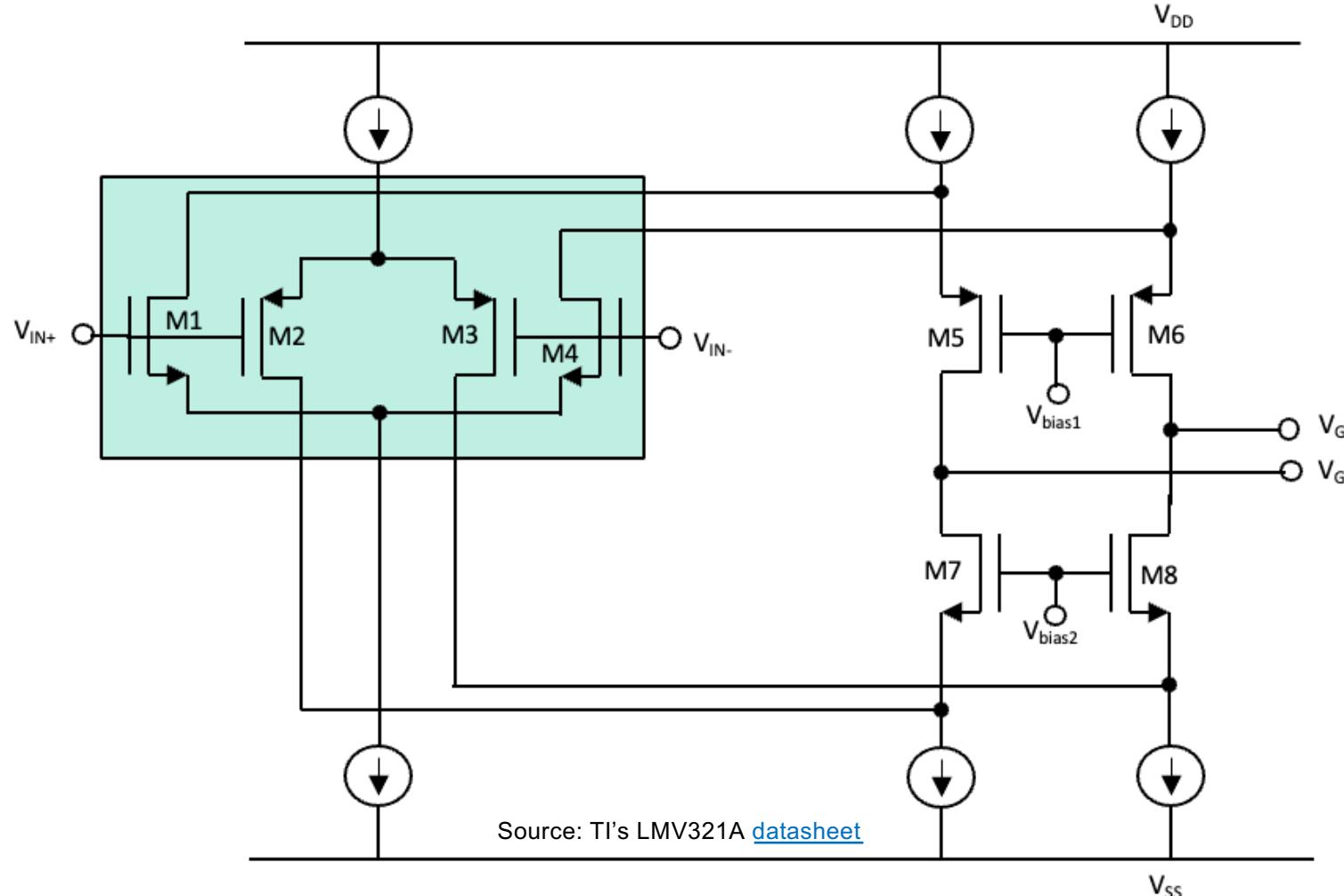
- ❖ Similar op-amp is obtained by:
  - Flip circuit up-side-down.
  - Replace all n-type with p-type and vice versa.

- Not rail-to-rail input or output.
- Asymmetrical output drive.
- Bad for low-voltage, single supply.



# Complementary differential input

- ❖ Use complementary differential input to solve input rail-to-rail issue.



Common-Mode Input Range	$V_{CMR}$	$V_{SS} - 0.3$	—	$V_{DD} + 0.3$	$V$
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Source: MCP6001 [datasheet](#)

# Op-amp Input Specifications

- These are the input specifications for the MCP6001 op-amp.

Input Offset						
Input Offset Voltage	$V_{OS}$	-4.5	—	+4.5	mV	$V_{CM} = V_{SS}$ (Note 1)
Input Offset Drift with Temperature	$\Delta V_{OS}/\Delta T_A$	—	$\pm 2.0$	—	$\mu V/^\circ C$	$T_A = -40^\circ C$ to $+125^\circ C$ , $V_{CM} = V_{SS}$
Power Supply Rejection Ratio	PSRR	—	86	—	dB	$V_{CM} = V_{SS}$

Input Bias Current and Impedance						
Input Bias Current:	$I_B$	—	$\pm 1.0$	—	pA	
Industrial Temperature	$I_B$	—	19	—	pA	$T_A = +85^\circ C$
Input Offset Current	$I_{OS}$	—	$\pm 1.0$	—	pA	
Common-Mode Input Impedance	$Z_{CM}$	—	$10^{13} \parallel 6$	—	$\Omega \parallel pF$	
Differential Input Impedance	$Z_{DIFF}$	—	$10^{13} \parallel 3$	—	$\Omega \parallel pF$	

Common-Mode						
Common-Mode Input Range	$V_{CMR}$	$V_{SS} - 0.3$	—	$V_{DD} + 0.3$	V	
Common-Mode Rejection Ratio	CMRR	60	76	—	dB	$V_{CM} = -0.3V$ to $5.3V$ , $V_{DD} = 5V$

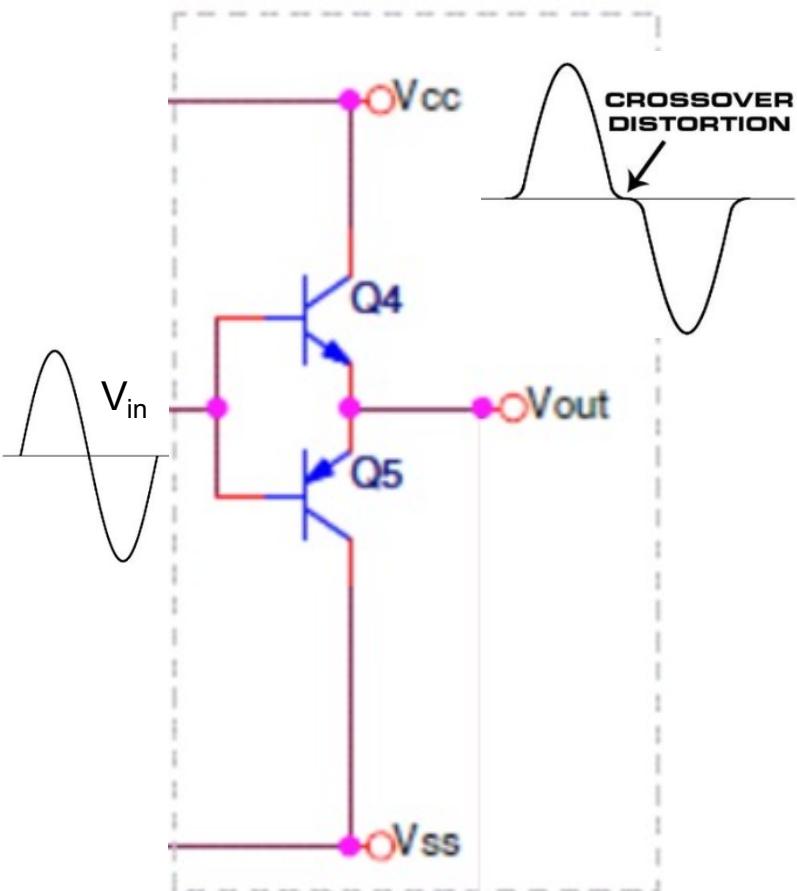


Highlighted entries are implemented in the MCP6001 LTSpice model.

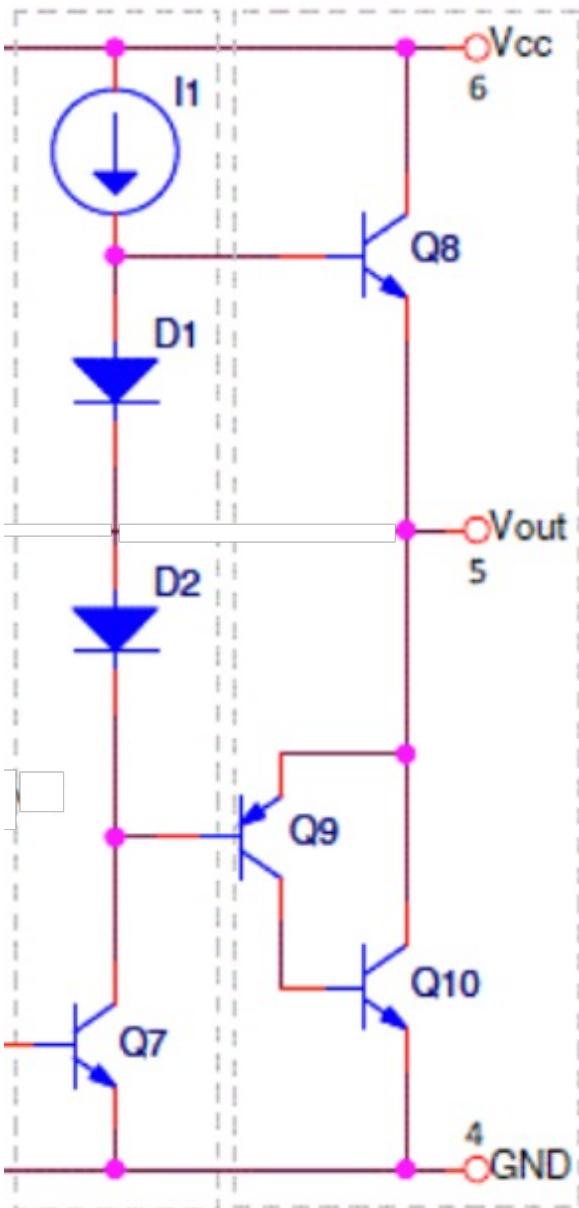
Source: MCP6001 [datasheet](#)

# Output Stage – Class B

- ❖ Yr 1<sup>st</sup> ADC part 2 Lecture 6, S3-5
- ❖ Q4 is emitter follower (Common-Emitter) for sourcing current to V<sub>out</sub> (PUSH)
- ❖ Q5 is another emitter follower for sinking current from V<sub>out</sub> (PULL)
- ❖ This is known as a PUSH-PULL or class B amplifier circuit
- ❖  $\delta V_{out} \approx \delta V_{in}$ , i.e. its gain is 1
- ❖ Each transistor only operate for half cycle or 180° of a sinewave signal
- ❖ Further, Q4 and Q5 requires V<sub>BE</sub> > 0.7V to start conducting, therefore this amplifier has distortion.

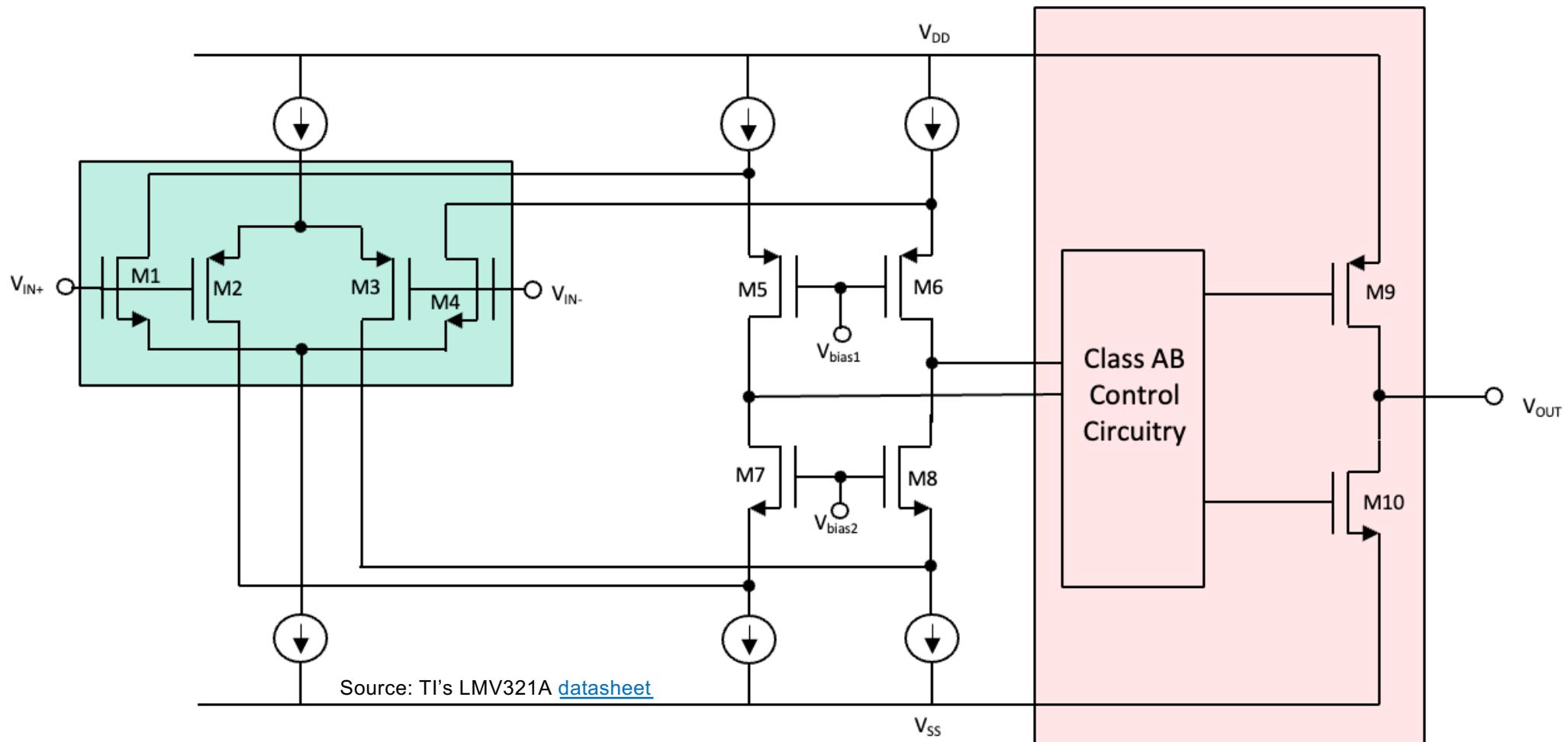


# Bipolar output Stage – Class AB output



- ❖ Q8 push emitter follower sourcing current
- ❖ Q9, Q10 pull emitter follower sinking current
- ❖ D1, D2 forward bias due to  $I_1$
- ❖ Keep Q8 and Q9 in linear region – reduce distortion
- ❖ Q9 PNP has poor current gain
- ❖ Combine with Q10 NPN to boost current gain
- ❖ Q9, Q10 - called a “**Sziklai**” pair (different from Darlington pair)
- ❖  $A_v \approx 1$

# Class AB output of MOSFET op-amp



- ❖ Improved output stage cannot drive low impedance load, say  $8\Omega$  speaker.

Output Short-Circuit Current (Source: MCP6001 <a href="#">datasheet</a> )	I <sub>SC</sub>	—	±6 ±23	—	mA mA	V <sub>DD</sub> = 1.8V V <sub>DD</sub> = 5.5V
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# Op-amp Output Specifications

- ❖ These are the output specifications for the MCP6001 op-amp.

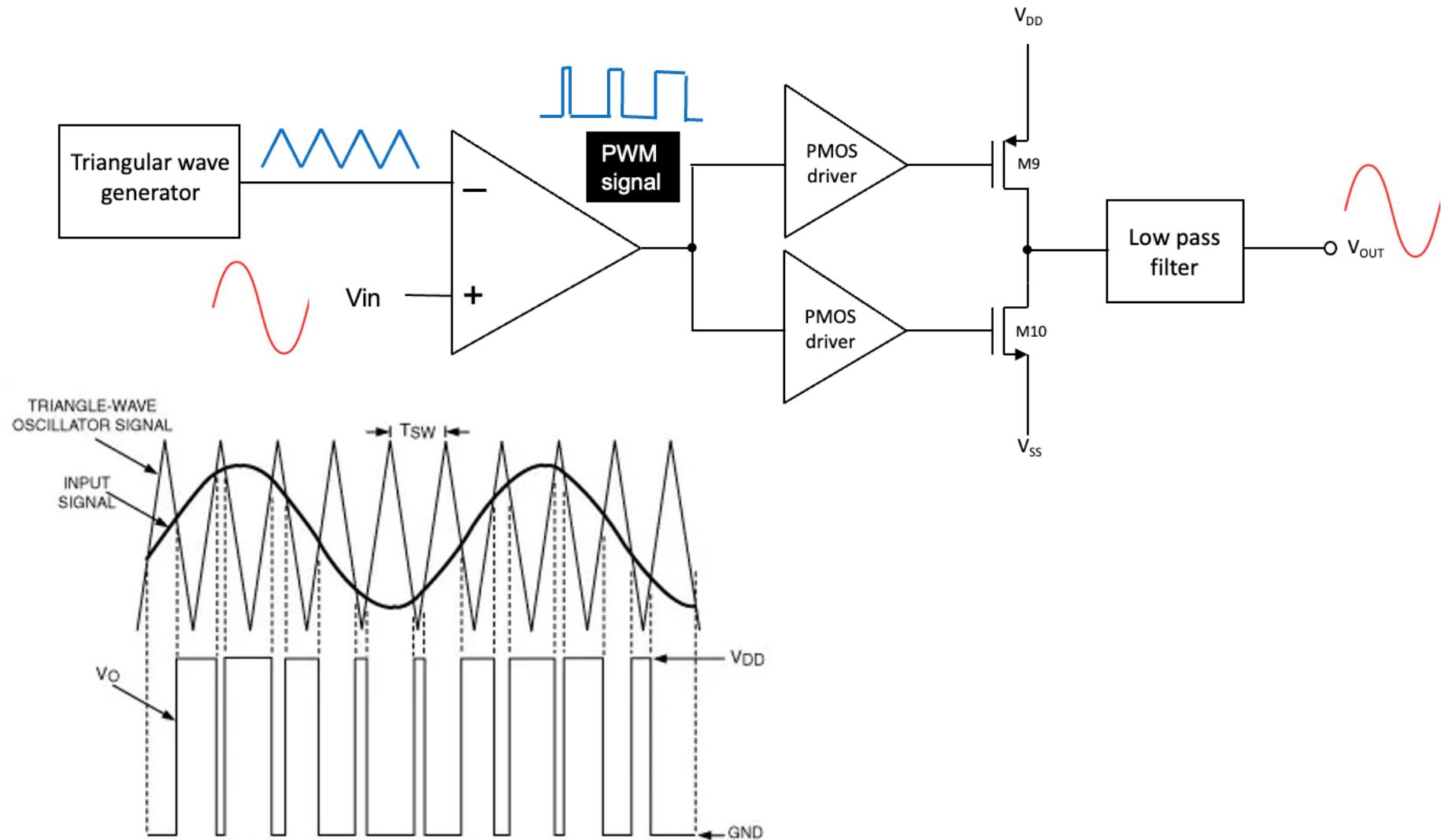
Output						
Maximum Output Voltage Swing	$V_{OL}, V_{OH}$	$V_{SS} + 25$	—	$V_{DD} - 25$	mV	$V_{DD} = 5.5V$ , 0.5V input overdrive
Output Short-Circuit Current	$I_{SC}$	— —	$\pm 6$ $\pm 23$	— —	mA mA	$V_{DD} = 1.8V$ $V_{DD} = 5.5V$



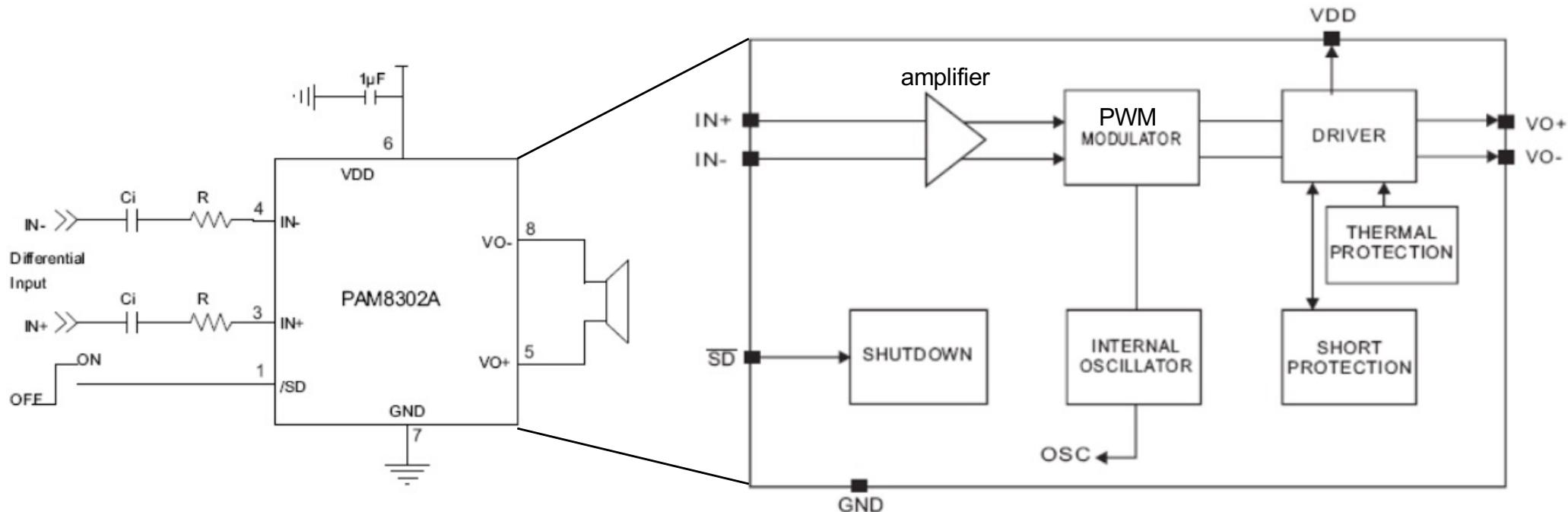
Highlighted entries are implemented in the MCP6001 LTSpice model.

Source: MCP6001 [datasheet](#)

# Block Diagram of a Class D amplifier



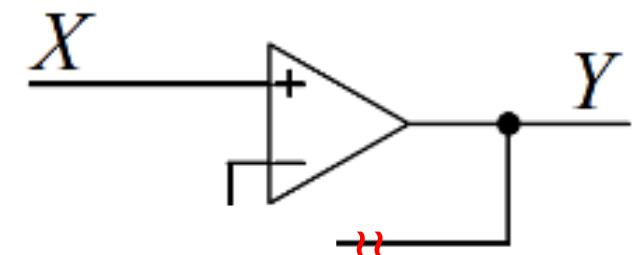
# The PAM8302A Audio Amplifier



- 2.5W Output at 10% THD with a  $4\Omega$  Load and 5V Power Supply
- Filterless, Low Quiescent Current and Low EMI
- High Efficiency up to 88%
- Superior Low Noise
- Short Circuit Protection

# Stability issue in op-amps

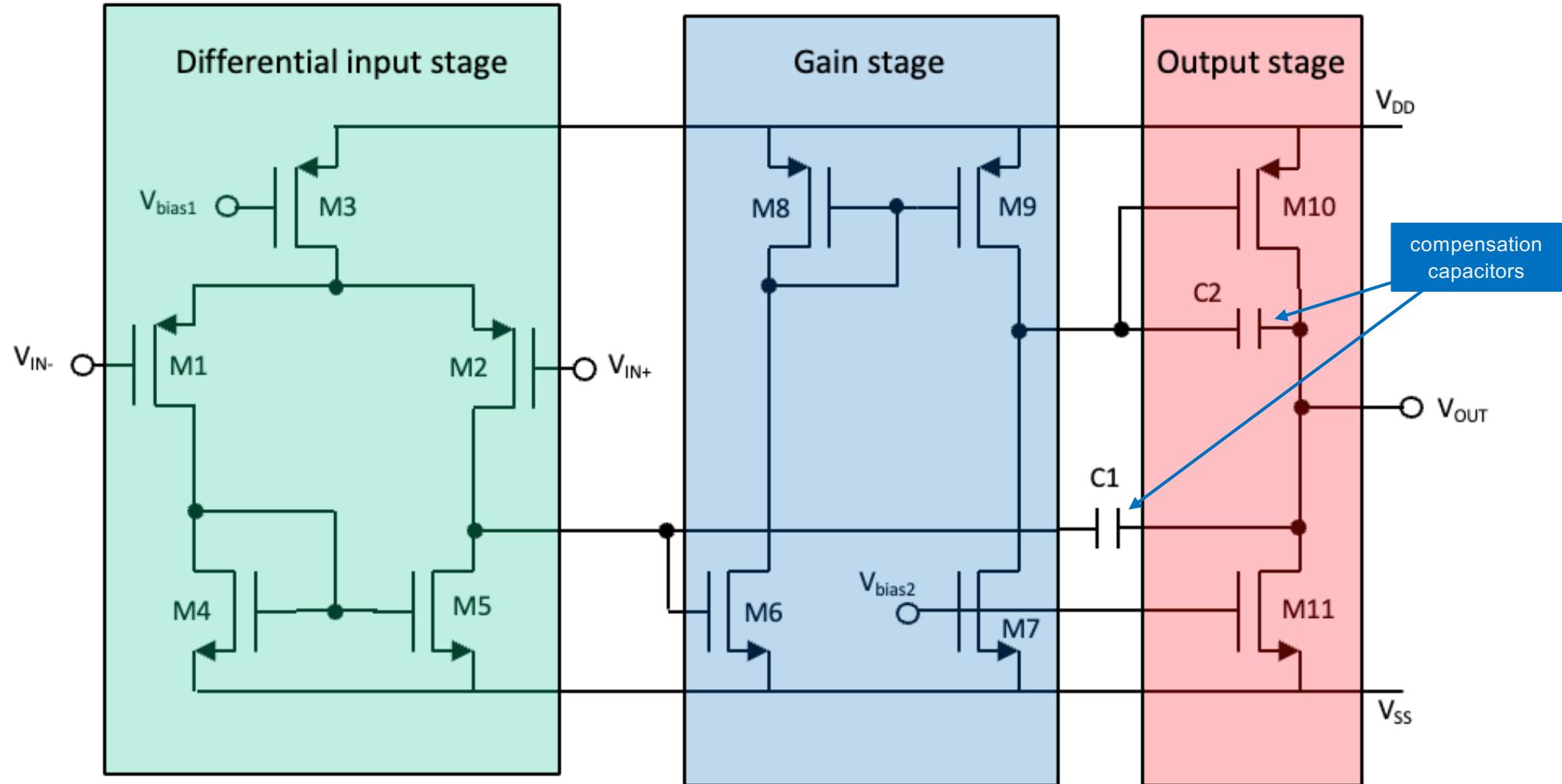
- ❖ Op-amp as an amplifier always uses NEGATIVE FEEDBACK to determine the gain.
- ❖ Consider this unity gain buffer: break the loop in the feedback path.
- ❖ Due to delay, could feedback a signal that is  $180^\circ$  out of phase relative to input.
- ❖ The negative feedback now become positive feedback, leading to oscillation.



## Stability requirement:

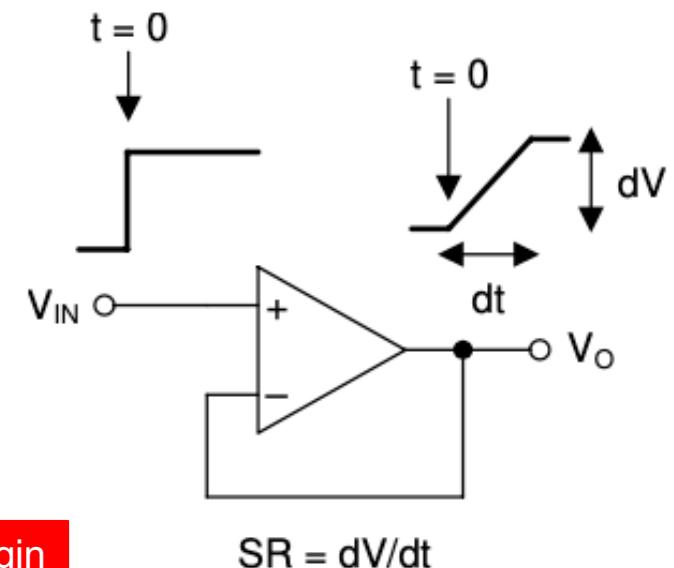
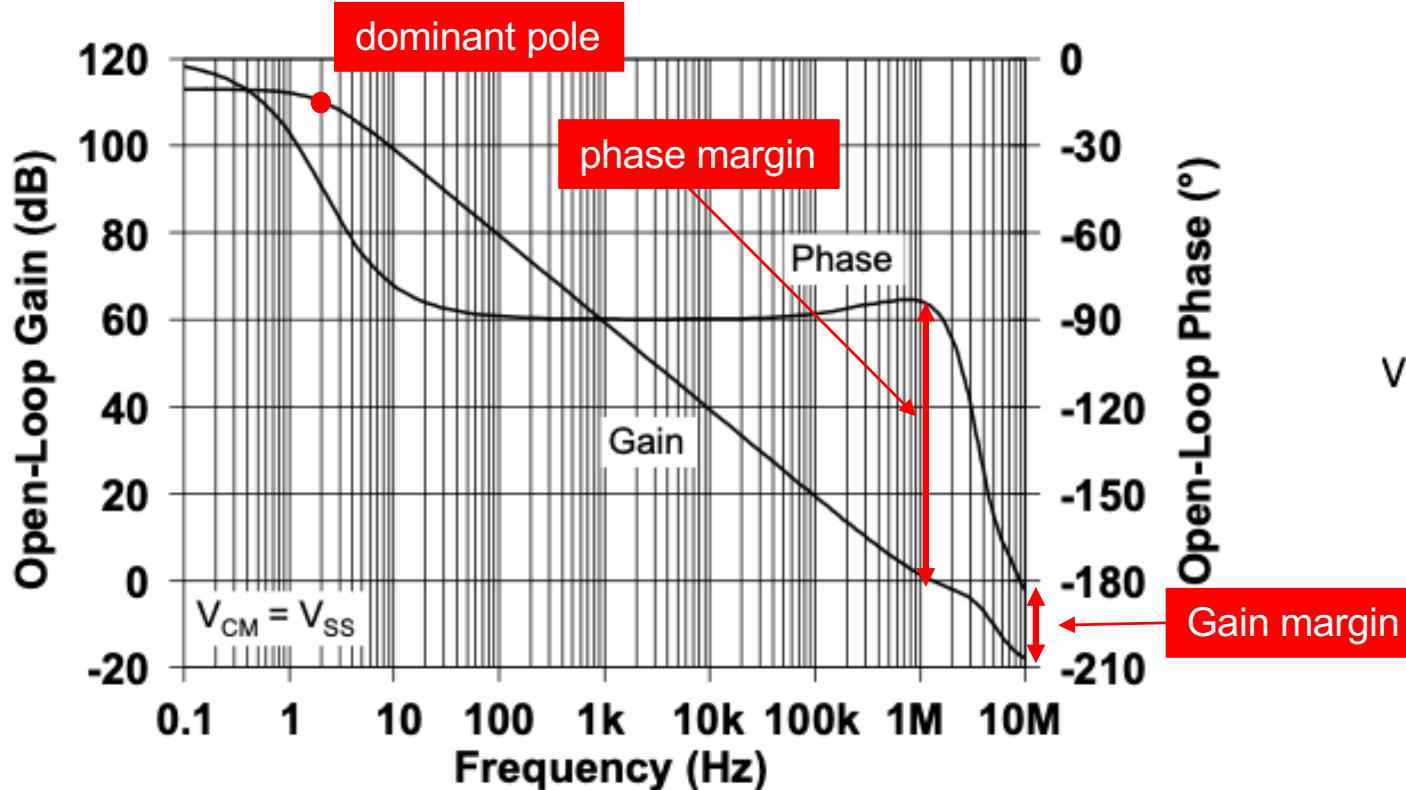
1. The open-loop **gain is  $> 1$** , but the **phase angle** must be  **$< 180^\circ$**  at all **signal frequencies**, OR
2. The **phase angle** is  **$\geq 180^\circ$** , but the open-loop **gain is  $< 1$**  at all **signal frequencies**.

# Open-loop gain and compensation capacitors



# Op-amp Loop Gain specification

Open-Loop Gain						
DC Open-Loop Gain (Large Signal)	$A_{OL}$	88	112	—	dB	$V_{OUT} = 0.3V \text{ to } V_{DD} - 0.3V$ , $V_{CM} = V_{SS}$
AC Response						
Gain Bandwidth Product	GBWP	—	1.0	—	MHz	
Phase Margin	PM	—	90	—	°	$G = +1 \text{ V/V}$
Slew Rate	SR	—	0.6	—	$\text{V}/\mu\text{s}$	



Source: MCP6001 [datasheet](#)